



Specifications

QwyitChip™

built on Intel® Arria V GX 150 MHz FPGA
(tested and available for verification)

- Encrypt or Decrypt with new key every 256 bits in a **single clock cycle**
 - 2 cycles combined
- Latency **6.67 nanoseconds** for Encrypt or Decrypt (combined, 13.34 ns)
- Throughput **64 Gbits/sec** (per 256-bits at 250MHz clock speed executing VHDL code)
 - **102.4 Gbps** on a Stratix V GX FPGA using a 100MHz clock speed executing Verilog code and 1024-bit Qwyit keys
- Less than **350 Source Lines of Verilog Code (SLOC)**
 - Significant space on chip available for other functions
- Qwyit is the first **native H/W encryption engine** – simpler, faster, more secure
- Mathematically provably secure

*See the video demonstration at Qwyit.com

Email info@qwyit.com to request a demo kit for your own verification

- QwyitChip™ is 1 primitive, 3 instructions (Select, Cipher, Update), 1 machine cycle
- FPGA space consideration is the only design constraint: key size can vary up to available space
- QwyitChip™ is the world's fastest Encryption Chip – **Nothing will ever be faster**
- **Hours versus years to encrypt daily internet content!**
- QwyitChip™ is 100% provably secure and **already Quantum Safe!**
- QwyitSDK™ operates identically in Software – speed limited only by configuration sizes